ABSTRACT OF THE DISCLOSURE

Increasing the retention time of an embedded dynamic random access memory (DRAM) is disclosed. An embedded DRAM includes a metal oxide semiconductor (MOS) capacitor. The capacitor has a storage node formed between a P+ doped region and a polysilicon plate within an N well. An N– doped region is situated substantially completely under the polysilicon plate and substantially under the P+ doped region. The presence of the N– doped region decreases the threshold voltage of the capacitor and reduces effectively the junction leakage current to the N well, achieving a larger retention time.